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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

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8

Please find below and/or attached an Office communication concerning this application or proceeding.

1

Office Action Summary	Application No.	Applicant(s)	
	09/733,597	BALMER ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9,11 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9 and 11* is/are rejected.

7)☒ Claim(s) *2 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-9, 11, and 17-19 have been examined.

Papers Received

2. Receipt is acknowledged of amendment papers submitted, where the papers have been placed of record in the file.

3. The amendment filed 02 February 2004 has successfully overcome the objections to the abstract and claims whereby the objections have been withdrawn.

Claim Objections

4. Claim 17 is objected to because of the following informalities: lines 3 and 10 state "a output," but should read "an output." In addition, lines 4 and 11 read "further including," but it is not immediately understood if the functional units or group include this limitation. The examiner is taking the lines to read, "the first (or second for line 11) functional unit group further includes" as hinted to by the multiplexer selecting between each functional unit of the group as stated later in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 12 recites the limitation "said instruction-selected one" in lines 7 and 14. There is insufficient antecedent basis for this limitation in the claim. The parent claim uses the limitation "instruction-specified" rather than "instruction selected" and as such, the examiner is taking claim 12 to mean to use the phrase given in claim 1.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor (6,266,766) in view of Dowling (6,170,051).

10. In regard to claim 1, O'Connor discloses a data processing apparatus comprising:

a. a register file (figure 1, 30) comprising a plurality of registers, each of said plurality of registers having a corresponding register number; In column 3, lines 37-39 show that there are register addresses and this means that there are multiple registers within the register file and a number to specify each.

a first functional unit (figure 1, 10) connected to said register file, said first functional unit responsive to an instruction to

i. receive data from one of said plurality of registers corresponding to an instruction-specified first operand register number at an operand input, Figure 1 shows that the functional unit receives at a first operand input data from the register file through a first operand register number (address, as shown above) and through the multiplexer (12).

ii. operate on said received data employing an instruction specified one of said first functional units, Column 2, lines 19-20 show that the functional unit outputs a result showing that it is operating on the data.

iii. output data to one of said plurality of registers corresponding to an instruction-specified first destination register number from an output; Figure 1 shows that the output of the functional unit is written back to the register file to a register specified by a register number (address, as shown above).

a second functional unit (figure 1, 20) connected to said register file, said second functional unit responsive to an instruction to

i. receive data from one of said plurality of registers correspondingto an instruction-specified second operand register number at an operand input, Figure 1 shows that the functional unit receives at an operand input data from the register file through another operand register number (address, as shown above) and through the multiplexer (22).

ii. operate on said received data employing an instruction-specified one of said second functional units, Column 2, lines 20-22 show that the functional unit outputs a result showing that it is operating on the data.

iii. output data to one of said plurality of registers corresponding to an instruction-specified second destination register number from an output; Figure 1 shows that the output of the functional unit is written back to the register file to a register specified by another register number (address, as shown above).

a first comparator (figure 2) receiving an indication of said first operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said first comparator indicating whether said first operand register number of said current instruction matches said second destination register number of said immediately preceding instruction (using figure 2, 60); Column 2, line 61 – column 3, line 12 gives the explanation of the comparison circuit of figure 2. The figure shows that the circuit receives an input for the current operand register number (address) and compares for a match with a second previous instruction destination register number (result return data path 26 register address) from the second functional unit (figure 1, 20). One can see that the path, 26, is indeed the feedback path from functional group two in figure 1.

a first register file bypass multiplexer (figure 1, 12) connected to said register file (30), said first functional unit group (10), said second functional unit (20) and said first comparator (figure 2), said first register file bypass multiplexer having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said output of said second functional unit and an output supplying an operand to said operand input of said first functional unit group (all shown in figure 1), said first multiplexer selecting said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and selecting said output of said second functional unit if said first comparator indicates a match. In column 2, lines 52-56, O'Connor shows that each multiplexer receives signals from a bypass control comparator circuit similar to that of figure 2. In column 3, lines 10-12, it is shown that if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit which will then select the data from the functional unit.

b. O'Connor does not disclose that the functional units are functional unit groups including a plurality of functional units. O'Connor also does not disclose said first functional units of said first functional unit group and said second functional units of said second functional unit group selected whereby functions often executed simultaneously within the same

instruction cycle have corresponding functional units placed in different functional unit groups and functions which are not often executed together within the same instruction cycle have corresponding functional units placed in the same functional unit group.

c. Dowling has disclosed the use of functional unit groups (also called sub-processors) that each have a plurality of functional units in column 1, line 67 – column 2, line 4. Column 11, lines 58-62 show that the sub-processors or functional unit groups execute instructions in lock step with the other sub-processors. Therefore, functional units are placed in different functional unit groups that often execute instructions simultaneously in the same cycle. Figure 3 shows an exemplary sub-processor and it is illustrated that this functional unit group executes instructions serially using the functional sub-units or functional units and not in parallel and thus functional units are placed within the functional groups to execute functions that do not occur simultaneously.

d. Column 1, line 65 – column 2, line 4 show that the processor with multiple functional unit groups is a VLIW processor. Column 1, lines 24-29 show that these multiple functional units (groups) allow for instruction level parallelism, which provides high performance VLIW processing as shown in lines 13-16. Also, column 1, lines 54-58 show that this VLIW structure has simple dispatch logic. This high performance and simple design would have motivated one of ordinary skill in the art to modify the

design of O'Connor to use multiple functional unit groups in the manner taught by Dowling.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor to use multiple functional unit groups as disclosed by Dowling so that high performance and simple design may be realized through the VLIW processing scheme taught by Dowling.

11. In regard to claim 5, O'Connor in view of Dowling discloses the data processing apparatus of claim 1, as described above, said first comparator (figure 2) further receiving an indication of said first destination register of said immediately preceding instruction (figure 2, result return data path 16 register address), said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction (using figure 2, 50), said first multiplexer further having a third input connected to said output of said first functional unit group (figure 1, 12), and said first multiplexer selecting said output of said first functional unit group if said first comparator indicates a match. Just as above, the comparator checks if the first destination register address matches the current operand source address. The first functional group output is selected if the register addresses do indeed match as described above.

12. In regard to claim 6, O'Connor in view of Dowling discloses the data processing apparatus of claim 1, as described above, said first functional unit group further responsive to an instruction to receive data from one of said plurality of registers corresponding to an instruction-specified third operand

register number at an operand input; The second input of the functional group (10) receives data from another register number through the multiplexer as shown in figure 1.

said apparatus further comprising:

a. a second comparator receiving an indication of said third operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said third operand register number of said current instruction matches said second destination register number of said immediately preceding instruction (using figure 2, 60); As described above, each multiplexer receives signals from a bypass control comparison circuit and thus with the addition of the multiplexer below, there is another comparator associated with it. As described above, the circuit compares the register address of the current instruction with the second destination address.

b. a second register file bypass multiplexer (figure 1, 14) connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said third operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said third operand input of said first functional unit group (all shown in figure 1),

said second multiplexer selecting said data from said register corresponding to said third operand number of said current instruction if said second comparator fails to indicate a match and selecting said second output of said second functional unit group if said second comparator indicates a match. As described above if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit, which will then select the data from the functional group.

13. In regard to claim 7, O'Connor in view of Dowling discloses the data processing apparatus of claim 6, as described above,

a. said first comparator further receiving an indication of said first destination register of said immediately preceding instruction (figure 2, result return data path 16 register address), said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said immediately preceding instruction (using figure 2, 50), said first multiplexer further having a third input connected to said first output of said first functional unit group (figure 1, 12), said first multiplexer selecting said first output of said first functional unit group if said first comparator indicates a match (done in same way as when the other bypass path is selected);

b. said second comparator further receiving an indication of said first destination register of said immediately preceding instruction (figure 2,

result data path 16 register address), said second comparator further indicating whether said third operand register number of said current instruction matches said first destination register number of said immediately preceding instruction(using figure 2, 50), said second multiplexer further having a third input connected to said output of said first functional unit group (figure 1, 12), and said second multiplexer selecting said output of said first functional unit group if said second comparator indicates a match (done in same way as when the other bypass path is selected).

14. In regard to claim 8, O'Connor in view of Dowling discloses the data processing apparatus of claim 1, as described above, further comprising:

a. a second comparator receiving an indication of said second operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said second operand register number of said current instruction matches said second destination register number of said immediately preceding instruction (using figure 2, 60); As described above, each multiplexer receives signals from a bypass control comparison circuit and thus with the addition of the multiplexer below, there is another comparator associated with it. As described above, the circuit compares the register address of the current instruction with the second destination address.

b. a second register file bypass multiplexer (figure 1, 22) connected to said register file, said first functional unit group, said second functional unit group and said second comparator, said second register file bypass multiplexer having a first input receiving data from said register corresponding to said second operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group (all shown in figure 1), said second multiplexer selecting said data from said register corresponding to said second operand number of said current instruction if said second comparator fails to indicate a match and selecting said output of said second functional unit group if said second comparator indicates a match. As described above if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit, which will then select the data from the functional group.

15. In regard to claim 9, O'Connor in view of Dowling discloses the data processing apparatus of claim 8, as described above, said second comparator further receiving an indication of said first destination register number of an immediately preceding instruction (figure 2, result return data path 16 register address), said second comparator indicating whether said second operand register number of said current instruction matches said first destination register number of said immediately preceding instruction (using element 60), said

second multiplexer further having a third input connected to said output of said first functional unit group (shown in figure 1, 22), and said second multiplexer further selecting said output of said first functional unit group if said second comparator indicates a match (using the generated comparison signal).

16. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Dowling as applied to claims 1 and 5-9 above, and further in view of Olson (5,123,108).

17. In regard to claim 3,

a. O'Connor in view of Dowling discloses the data processing apparatus of claim 1, as described above, wherein said first comparator further receives an indication of said second destination register number of a second preceding instruction (figure 2, result return data path 26 register address), said first comparator further indicating whether said first operand register number of said current instruction matches said second destination register number of said second preceding instruction (using figure 2, 60), and wherein said multiplexer further has a third input (figure 1, 12).

b. O'Connor in view of Dowling does not disclose that the apparatus is further comprising an output register having an input connected to output of functional unit group and an output connected to said register file for temporarily storing said output of said second functional unit group prior to storing in said register corresponding to said destination register number, wherein said multiplexer has an input connected to said output

register output, said multiplexer selecting said output register output if said first comparator indicates a match.

c. Olson discloses a data processing apparatus with register bypassing (figure 2) further comprising an output register (figure 2, 28a) having an input connected to the output of the functional unit and an output connected to said register file for temporarily storing said output of function unit prior to storing in said register corresponding to said destination register number (address), wherein multiplexer (figure 2, 18) has an input connected to said output register output, said multiplexer selecting output register output if comparator (figure 2, 24) indicates a match (column 4, lines 6-16).

d. The output register given by Olson has numerous desirable qualities. First, one can be sure that the correct data is being written to the register file because the output register will hold the data throughout the clock cycle. Also, using the register in conjunction with the disclosure of O'Connor allows for the retention of preceding data for another clock cycle, which is used by the multiplexer on a third input for extended bypassing capabilities.

e. This increased data integrity for the register file and the ability to have more data readily available for bypassing purposes would have motivated one of ordinary skill in the art to incorporate the teaching of Olson's output register into the design of O'Connor in view of Dowling.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Dowling to include the output register specified by Olson in order to have high data integrity in the register file and to have more data available for register bypassing purposes.

18. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Deao (5,970,241) and further in view of Dowling

19. In regard to claim 11,

a. O'Connor discloses a data processing apparatus comprising:

i. a first register file (figure 1, 30) comprising a plurality of registers, each of said plurality of registers having a corresponding register number; In column 3, lines 37-39 show that there are register addresses and this means that there are multiple registers within the register file and a number to specify each.

ii. a first functional unit group (figure 1, 10) including an input connected to said register file, an output connected to said register file, and a plurality of first functional units, said first functional unit group responsive to an instruction to

(1) receive data from one of said plurality of registers in said register file corresponding to an instruction-specified first operand register number at an operand input; Figure 1 shows that the functional unit group receives at a first operand input data from the register file through a first

operand register number (address) and through the multiplexer (12).

(2) operate on said received data employing an instruction specified one of said first functional units; Column 2, lines 19-20 show that the functional unit group outputs a result showing that it is operating on the data.

(3) output data to one of said plurality of registers in said register file corresponding to an instruction specified first destination register number from an output; Figure 1 shows that the output of the functional unit group is written back to the register file to a register specified by a register number (address).

iii. a second functional unit group (figure 1, 20)including an input connected to said register file, an output connected to register file, and a plurality of second functional units, said second functional unit group responsive to an instruction to

(1) receive data from one of said plurality of registers in said register file corresponding to an instruction-specified second operand register number at an operand input; Figure 1 shows that the functional unit group receives at an operand input data from the register file through another operand register number (address) and through the multiplexer (22).

(2) operate on said received data employing an instruction specified one of said second functional units; Column 2, lines 19-20 show that the functional unit group outputs a result showing that it is operating on the data.

(3) output data to one of said plurality of registers in said register file corresponding to an instruction-specified second destination register number from an output; Figure 1 shows that the output of the functional unit group is written back to the register file to a register specified by another register number (address).

iv. a first path connecting said register file to first functional unit group comprising

(1) a first comparator (figure 2), wherein, said comparator receives an indication of said first operand register number of a current instruction and an indication of said second destination register number of a preceding instruction, and said first crosspath comparator indicates whether said first operand register number of said current instruction matches said second destination register number of said preceding instruction (using figure 2, 60); Column 2, line 61 – column 3, line 12 gives the explanation of the comparison circuit of figure 2. The figure shows that the circuit receives an input for the current operand register number (address) and

compares for a match with a second previous instruction destination register number (result return data path 26 register address) from the second functional unit (figure 1, 20). One can see that the path, 26, is indeed the feedback path from functional group two in figure 1.

(2) a first multiplexer (figure 1, 12) connected to said register file (30), said first functional unit group (10), said second functional unit group (20) and said first comparator (figure 2), said first multiplexer having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said output of said second functional unit group and an output supplying an operand to said operand input of said first functional unit group (all shown in figure 1), wherein, said first multiplexer selects said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and selects said output of said second functional unit group if said first comparator indicates a match. In column 2, lines 52-56, O'Connor shows that each multiplexer receives signals from a bypass control comparator circuit similar to that of figure 2. In column 3, lines 10-12, it is shown that if current operand register number (address) is the same as

the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit which will then select the data from the functional group.

b. O'Connor does not disclose

i. a second register file comprising a plurality of registers,

ii. both functional groups being connected to both register files;

iii. the first path being a crosspath where the first comparator checks if the first operand register is in the second register file.

iv. the functional units are functional unit groups including a plurality of functional units.

O'Connor also does not disclose said first functional units of said first functional unit group and said second functional units of said second functional unit group selected whereby functions often executed simultaneously within the same instruction cycle have corresponding functional units placed in different functional unit groups and functions which are not often executed together within the same instruction cycle have corresponding functional units placed in the same functional unit group.

c. Deao has disclosed in figure 2:

i. a second register file (20b) comprising a plurality of registers;

ii. both functional groups (L1,S1,M1,D1, and L2,S2,M2,D2) being connected to both register files (by crosspaths 1x and 2x);

iii. the first path being a crosspath where the first comparator checks if the first operand register is in the second register file. Deao shows the crosspath (1x) from the second register file (20b) where the multiplexer shown then selects the appropriate register file to select from depending on where the correct operand is.

Dowling has disclosed the use of functional unit groups (also called sub-processors) that each have a plurality of functional units in column 1, line 67 – column 2, line 4. Column 11, lines 58-62 show that the sub-processors or functional unit groups execute instructions in lock step with the other sub-processors. Therefore, functional units are placed in different functional unit groups that often execute instructions simultaneously in the same cycle. Figure 3 shows an exemplary sub-processor and it is illustrated that this functional unit group executes instructions serially using the functional sub-units or functional units and not in parallel and thus functional units are placed within the functional groups to execute functions that do not occur simultaneously.

d. The crosspath and second register file of Deao provides for increased quantity and flexibility in nearby available data. Having more data in local registers means quicker data access because of the close proximity and faster access time of registers. Column 1, line 65 – column

2, line 4 show that the processor with multiple functional unit groups is a VLIW processor. Column 1, lines 24-29 show that these multiple functional units (groups) allow for instruction level parallelism, which provides high performance VLIW processing as shown in lines 13-16. Also, column 1, lines 54-58 show that this VLIW structure has simple dispatch logic.

e. This high performance and simple design would have motivated one of ordinary skill in the art to modify the design of O'Connor to use multiple functional unit groups in the manner taught by Dowling. The increased quantity and flexibility of quickly accessible data given by Deao would have motivated one of ordinary skill in the art to incorporate the given design of Deao for crosspaths into O'Connor.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor to include the second register file and crosspath design given by Deao in order to gain greater capacity and flexibility of quickly accessible data as well as to include the multiple functional unit groups of Dowling so a high performance and simple design may be realized through the VLIW processing scheme of Dowling.

Response to Arguments

20. Applicant's arguments with respect to claims 1-3, 5-9, and 11 have been considered but are moot in view of the new ground(s) of rejection.

21. The examiner would like to point out that in the argument for claim 3, Applicant's representative has stated a portion of Olson that does not read on the

limitation in question. The examiner made the rejection to that limitation of claim 3 based on a citation of O'Connor (which has not been descriptively argued) and not Olson. The examiner is not required to show this limitation in the Olson reference since this reference is used to provide a different limitation of the claim and motivation for introducing that limitation.

Allowable Subject Matter

22. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically teach *only* providing operands to a functional unit via a read operation in a pipeline stage as the first half of operation of the functional unit and *only* a register write operation of a result in a second stage for the second half of operation of the functional unit where the sum of time for these half-operations is equal to that of the first and second halves of operation of the slowest functional unit. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record to *only* provide operands to a functional unit via a read operation in a pipeline stage as the first half of operation of the functional unit and *only* perform a register write operation of a result in a second stage for the second half of operation of the functional unit where the sum of time for these half-operations is equal to that of the first and second halves of operation of the slowest functional unit.

23. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically teach the use of an output multiplexer having a plurality of inputs receiving respective outputs of said functional units and an output, said output multiplexer selecting said output of said instruction-selected one of said functional units for each functional unit group. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record to make use of an output multiplexer having a plurality of inputs receiving respective outputs of said functional units and an output, said output multiplexer selecting said output of said instruction-selected one of said functional units for each functional unit group since the functional units of the groups operate serially as in figure 3.

24. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically teach the data processing apparatus of claim 2. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record to teach the data processing apparatus of claim 2.

25. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record

does not specifically teach the use of an output multiplexer having a plurality of inputs receiving respective outputs of said functional units and an output, said output multiplexer selecting said output of said instruction-selected one of said functional units for each functional unit group. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record to make use of an output multiplexer having a plurality of inputs receiving respective outputs of said functional units and an output, said output multiplexer selecting said output of said instruction-selected one of said functional units for each functional unit group since the functional units of the groups operate serially as in figure 3.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the date of this final action.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited in the previous action remain pertinent to the disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
April 16, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100